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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/766,798	01/22/2001	Jamin Ling	5833-A-13	8425

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EXAMINER	
NGUYEN, THINH T	#3
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/05/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/766,798	LING ET AL.	
	Examiner	Art Unit	
	Thinh T Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☒ Claim(s) *14-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED OFFICE ACTION

Specification

1. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant cooperation is requested in correcting any errors of which the applicant may become aware in the specification.

Claims Objections

2. Claim 14,15,16,17,18,19,20,21,22,23 and 24 are all objected to since in those claims, the applicants say they are dependant on claim 14 when they mean claim 13. Corrections or clarifications are required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1,2,3,4,5,6,7,8,9,10,11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al. (U.S. patent 6077723) in view of Hosomi et al.

(U.S. patent 5747881), Andricacos et al (U.S. patent 5937320) and in view of further remark.

REGARDING TO CLAIM 1

Farnworth et al. (US patent 5747881) disclose the invention of an integrated circuit structure that have in combination:

A semiconductor wafer (fig 1 and fig 2 numeral 16) having an upper surface, the semiconductor wafer having a plurality of identical die (fig 1 numeral 18) formed inside, each of the identical die having a plurality of semiconductor devices formed on the surface of the semiconductor wafer; a patterned layer of interconnect metal (fig 2 layer 32) formed upon the upper surface of the semiconductor wafer for electrically interconnecting the plurality of semiconductor devices formed within each such die, the patterned layer of interconnect metal including connection pads (fig 2 layer 26) for making electrical connection to circuitry external to the semiconductor wafer.

Even though Farnworth do not mention the formation of triple metal layers to form the bump electrodes, Hoshomi et al. in their invention disclose a semiconductor device with bump electrodes that have a patterned layer (fig 1 layer 2) of interconnect metal formed upon the upper surface of the semiconductor wafer for electrically interconnecting the plurality of semiconductor devices formed within each such die with the patterned layer of interconnect metal including connection pads for making electrical connection to circuitry external to the semiconductor wafer. a patterned layer of nickel plated (fig 1 layer 5b) over each connection pad for mechanically and electrically bonding to the interconnect metal forming such connection pad; a patterned layer of palladium (fig 1 layer 5c)plated over the patterned layer of nickel

above each connection pad for preventing the nickel from diffusing outwardly through the palladium and a patterned layer of gold (fig 1 layer 6) plated over the patterned layer of palladium above each connection pad to facilitate the joint of such connection pad with a connection element.

It would be obvious for a person of ordinary skill in the art at the time the invention was made, to use the teachings of Farnworth et al. and Hosomi et al. in order to fabricate

An integrated circuit structure that have in combination:

a. a semiconductor wafer with an upper surface, the semiconductor wafer includes a plurality of identical die formed therein, each of the identical die having a plurality of semiconductor devices formed on the surface of the semiconductor wafer.

b. a patterned layer of interconnect metal formed upon the upper surface of the semiconductor wafer for electrically interconnecting the plurality of semiconductor devices formed within each such die with the patterned layer of interconnect metal having connection pads for making electrical connection to circuitry external to the semiconductor wafer.

c. a patterned layer of nickel plated over each connection pad for mechanically and electrically bonding to the interconnect metal .

d. a patterned layer of palladium plated over the patterned layer of nickel above each connection pad for preventing the nickel from diffusing outwardly through the palladium

e. a patterned layer of gold plated over the patterned layer of palladium above each connection pad to facilitate the joint of such connection pad with a connection element.

The reasoning is as follow:

A person of ordinary skill in the art would have been motivated to use the right technique and the right material as taught by Farnworth et al. and Hosomi et al. in order to built the right metallization structure to form the connection within and outside of the semiconductor die.

REGARDING TO CLAIM 2,3,4 AND 5

The selection of connection element such as gold bump, gold wire bond, solder bump, nickel bump is old and well known and is considered routine ordinary skill in the art.

REGARDING TO CLAIM 6

Hoshomi et al. has a Nickel layer (fig 1 layer 5b) on top of the patterned layer of Interconnect metal.

REGARDING TO CLAIM 7,8,9 AND 10

The selection of connection pads pitch and the thickness of different layer of Nickel, Palladium, and Gold is just ordinary routine design choice of the art

REGARDING TO CLAIM 11

Andricacos et al. has the interconnect layer (fig 1 layer 12) made of copper.

REGARDING TO CLAIM 12.

Hosomi et al. (fig 1 layer 2) has the interconnect layer 2 made of Aluminum.

5. Claims 13,14,15,16,17,18,19, 20, 21,22,23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al. (U.S. patent 6077723) in view of Hosomi et al. (U.S. patent 5747881) , Andricacos et al (U.S. patent 5937320) and in view of further remark.

REGARDING CLAIM 13

Farnworth et al. (US patent 5747881) disclose the method of fabrication of an integrated circuit structure that have in combination:

A semiconductor wafer (fig 1 and fig 2 numeral 16) having an upper surface, the semiconductor wafer having a plurality of identical die (fig 1 numeral 18) formed inside, each of the identical die having a plurality of semiconductor devices formed on the surface of the semiconductor wafer; a patterned layer of interconnect metal (fig 2 layer 32) formed upon the upper surface of the semiconductor wafer for electrically interconnecting the plurality of semiconductor devices formed within each such die, the patterned layer of interconnect metal including connection pads (fig 2 layer 26) for making electrical connection to circuitry external to the semiconductor wafer.

Hoshomi et al. in their invention disclose a semiconductor device with bump electrodes that have a patterned layer (fig 1 layer 2) of interconnect metal formed upon the upper surface of the semiconductor wafer for electrically interconnecting the plurality of semiconductor devices formed within each such die with the patterned layer of interconnect metal including connection pads for making electrical connection to circuitry external to the semiconductor wafer. A patterned layer of nickel plated (fig 1 layer 5b) over each connection pad for mechanically and electrically bonding to the interconnect metal forming such connection pad; a patterned layer of palladium (fig 1 layer 5c)plated over the patterned layer of nickel above each connection pad for preventing the nickel from diffusing outwardly through the palladium and a patterned layer of gold (fig 1 layer 6) plated over the patterned layer of palladium above each connection pad to facilitate the joint of such connection pad with a

connection element.

Although Hosomi et al. do not mention the method of fabrication the contact bumps structure with the formation of multiplayer Ni , Pd and Au using electro less plating;Andricacos et al. (fig 1 layer 16,18,20) do use electro less plating or electroplating to deposit several layers of metal to form the desired structure

It would have been obvious to one of ordinary skill in the art the time the invention was made to use the teachings of Farnworth et al., Hosomi et al. and Andricacos et al. in order to formulate a process of fabrication of a semiconductor device with the formation of connection pads on a plurality of integrated circuit die formed in a semiconductor wafer, the semiconductor wafer having an upper surface, each of the integrated circuit die having a plurality of semiconductor devices formed therein upon the surface of the semiconductor wafer, This process will include the steps of:

a. forming a patterned layer of interconnect metal upon the upper surface of the semiconductor wafer for electrically interconnecting the plurality of semiconductor devices formed within each such integrated circuit die, patterned layer of interconnect metal including connection pads for making electrical connection to circuitry external to the semiconductor wafer;

b. following step a., forming a patterned layer of nickel by electroless plating over each connection pad for mechanically and electrically bonding to the interconnect metal at each such connection pad;

c. following step b., forming a patterned layer of palladium by electroless plating over the patterned layer of nickel above each connection pad for preventing the nickel from

diffusing outwardly through the palladium during subsequent heating cycles; and

d. following step c., forming a patterned layer of gold by electroless plating over the patterned layer of palladium above each connection pad to facilitate the joint of such connection pad with a connection element.

The reasoning is as follow:

A person of ordinary skill in the art would have been motivated to use the right technique and the right material as taught by Farnworth et al. and Hosomi et al. in order to formulate a method to built the right metallization structure to form the connection within and outside of the semiconductor die.

REGARDING TO CLAIM 14,15,16,17 AND 18

The process of joining gold bump, gold wire bond, solder bump, Nickel bump and Nickel plated on top of the patterned layer at each connection pads are consider within The skill of a person with routine ordinary knowledge in the art.

REGARDING TO CLAIM 19,20,21, AND 22

The selection of connection pads pitch and the thickness of different layer of Nickel, Palladium, and Gold is just ordinary routine design choice.

REGARDING CLAIM 23.

Andricacos et al. has the interconnect layer (fig 1 layer 12) made of copper.

REGARDING CLAIM 24

The step of heating the semiconductor after a process is considered of ordinary routine skill in the art.

6. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

7. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

CONCLUSION

8. The prior arts made of record and not relied upon are considered pertinent to applicant disclosure:

Kondo et al. (US patent 5656858) disclose a semiconductor device with bump Structure.

Budnaitis (US patent 5766979) discloses a wafer level contact sheet and assembly.

Farnworth et al. (US patent 5801452) disclose a multi-chip module including semiconductor wafer or dice interconnect substrate, and alignment member.

Iwabuchi (US patent 6008543) discloses a conductive bumps on pads for flip chip Application.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose phone number is (703) 305-0421. The Examiner can normally be reached on Monday to Friday from 8.30 A.M. to 5.00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, David C. Nelms can be reached on (703) 308-4910. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thinh T. Nguyen TTN

Art Unit 2818

David Nelms
Supervisory Patent Examiner
Technology Center 2800